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Metastability and Comparative Analysis of Sequential Circuit using CNTFET and MOSFET

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Abstract: Metastability occurs when signals are transferred between asynchronous clock domains. In today's modern world where everything is digitized and miniaturized we need small and stable digital system for years. The circuit failure largely depends upon metastable state in digital circuits. This can be avoided by using synchronizer. The goal of the proposed work is to design a synchronizer with both CNTFET and MOSFET technology and simulate in HSPICE with 32nm scale. This paper presents how the metastability response in terms of MTBF, Noise margin, power, Delay and Power Delay Product (PDP) parameters are better in CNTFET based synchronizer as compare to MOSFET. The simulation results show that circuits designed using CNTFETs have a high robustness to voltage and temperature variations as compared to MOSFET based circuits**.** Also due to variation in voltage and temperature in CNTFET give no or very less variation in PDP. This paper will confirm that CNTFET technology is a viable solution to replace conventional MOSFET technology and it turns out to be an effective choice of future technology if manufacturability issues such as controllability of metallic/semiconducting property and metallic contacts are taken care of.

Keywords: CNTFET, MTBF, Sequential Circuits, MOSFET, PDP, Noise Margin

1. INTRODUCTION

Scaling down the size of CMOS technology in nano ranges can result in the following problems: short channel effects (SCEs), high-power densities and reduced gate control and high sensitivity to method modifications. Due to the mention reasons, scientists have done studies in nanotechnologies such as Single Electron Transistor (SET), Quantum-dot Cellular Automata (QCA), and Carbon Nanotube Field Effect Transistor (CNFET). Among them Carbon Nanotube Field Effect Transistor (CNFET) be caused of their most similarities with MOSFET technology came under more consideration.[1-2] To outline noticeable characteristics of CNFET are lower power consumption compared to MOSFET, higher efficiently and P-CNFET and N-CNFET, which having the same device geometries and mobilities and subsequently, the same current drive abilities, essential for transistor sizing in the complex circuits They are most preferred over the other complement traditional silicon technology due to three reasons: first, the operation principle and the device structure are similar to CMOS devices; we can reuse the established CMOS design infrastructure, second, we can reuse CMOS fabrication process[3]. Also the most important reason is that CNTFET has the best experimentally demonstrated device current carrying ability today.Significant advances have been achieved in understanding device physics and improving the device performance for carbon nanotube field effect transistors. One of the basic ideas is to replace the silicon MOSFETs with CNTFETs, which should overcome all the limitations of silicon MOSFETs such as the exponential increase of leakage currents in scaled devices. The limits can be overcome to some extent and facilitate the further scaling down of device dimensions by modifying the channel material in the traditional MOSFET structure with a single carbon nanotube. Much progress has been made in recent years showing that CNT based FETs can outperform the state of the art silicon FETs in many ways. Although CNT has less reliability and greater cost problem, it can play a vital role in nano electronic devices such as transistors, memory components etc. because of its excellent electrical conductivity and high dielectric properties. Therefore, Field Effect Transistors have been tried to be constructed from CNT to surmount the limitations of Si-MOSFET such as carrier mobility, channel length, ballistic conduction, trans-conductance, heat dissipation, threshold voltage etc. [4]

Methodology:

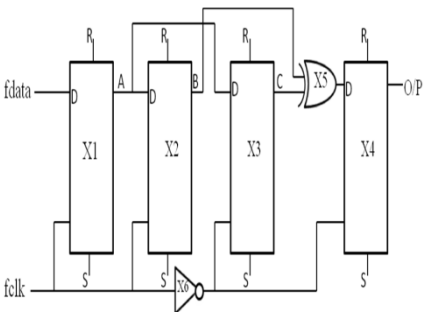

Figure 1: Sequential circuit made using CNTFET and MOSFET [5-6]

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Figure 1 shows block diagram of sequential circuit, which is implemented using MOSFET and CNTFET in 32nm technology. Performance of both the circuits is compared using metrics. The metrics calculated are Average Power Consumption, Delay, Power-Delay Product, Noise Margin and MTBF.

Whenever a clocked flip-flop synchronizes input, there is a small probability that the flip-flop output exhibit an unpredictable delay. This happens when the input transistion not only voilates the setup and hold-time specifications, but actually occurs within the tiny timing window where the flip-flop accepts the new input.[7] Under these circumstances, the flip- flop enter a symmetrically balanceed transitory state called metastable(meta = between). Therefore, it is required to calculate the time window, Td for the calculation of MTBF. Td, is the time window in which the output becomes stable again after metastable state.

For calculation of MTBF in sequential circuits,
MTBF= 1/(Td*fclk*fdata) (1)
Where, Td is critical time window, fclk is frequency of clock and fdata is input data frequency. [8]

For calculation of Noise Margin:
Noise margin is a parameter closely related to the input-output voltage characteristics. This parameter allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected. The specification most commonly used to specify noise margin (or noise immunity) is in terms of two parameters- The LOW noise margin, NML, and the HIGH noise margin, NMH. NML is defined as the difference in magnitude between the maximum LOW output voltage of the driving gate and the maximum input LOW voltage recognized by the driven gate.

Noise margin high and low are calculating using the following formula
NMH = Voh - Vih (2)
and

NML = Vol – Vil (3)

Where, Vih and Vil, smallest values when slope is -1 and Voh and Vih represent largest value when slope is -1. [9]
For Calculation of PDP:
The power–delay product is a figure of merit correlated with the energy efficiency of a logic gate or logic family. Also known as switching energy, it is the product of power consumption (averaged over a switching event) times the input–output delay, or duration of the switching event. [10]

PDP = Power * Delay (4)

Simulation Analysis and Results:
Metastability Analysis:
Figure 2 shows calculated MTBF in implementing Synchronizer using CNTFET and MOSFET. It represents that higher stability in CNTFET and a lower critical time window.

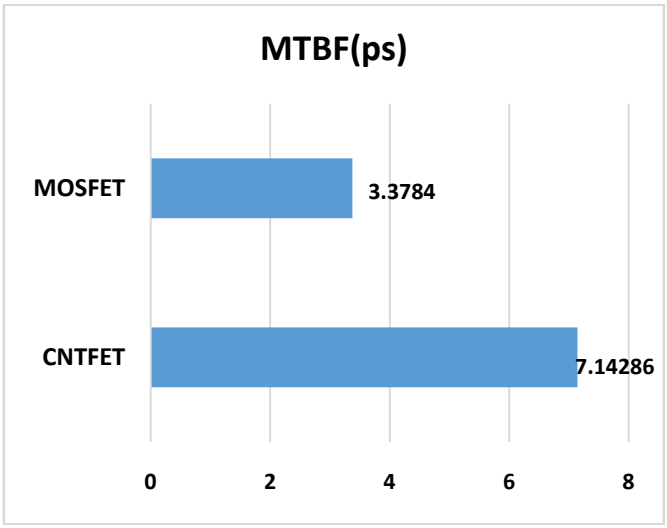

Figure 2: MTBF Analysis

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Noise Margin:
Figure 3 and Figure 4 shows Noise Margin in implementing Synchronizer using CNTFET and MOSFET. It shows better performance in NMH and equal NML in CNTFET on the basis of Noise Immunity.

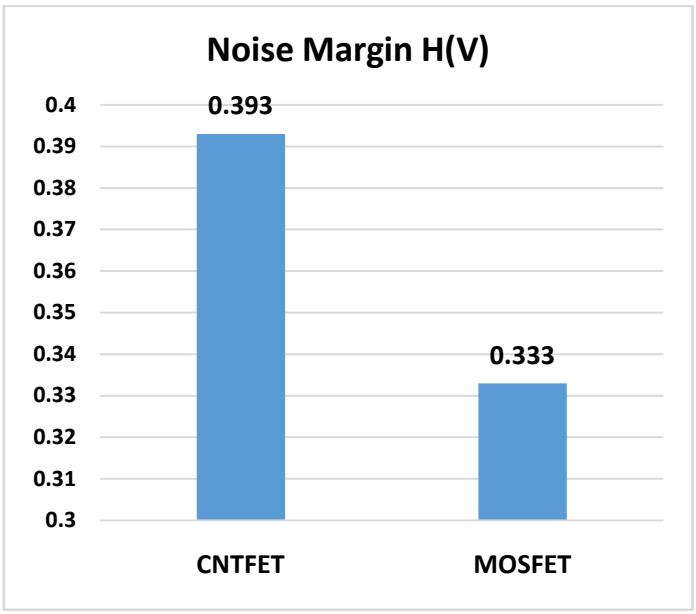

Figure 3: Noise Margin High

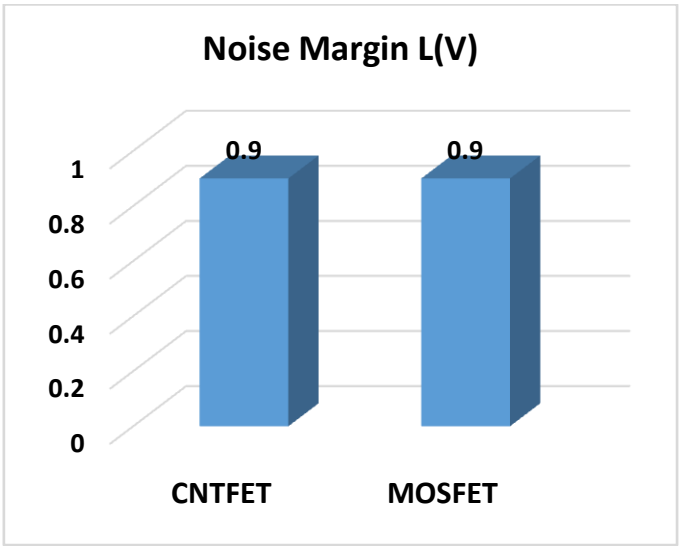

Figure 4: Noise Margin Low

PDP Variation:
Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile environments, reduction of delay and power consumption is very challenging. MOSFET and CNTFET can be compared using the PDP as metric. Table 1 shows the delay, power, and PDP of synchronizer in 32 nm MOSFET and 32 nm CNTFET technologies; the PDP of the 32 nm MOSFET is about 1000 times higher than that of the 32 nm CNTFET.

Table 1: Delay, Power and PDP measurement of synchronizer.

Device	Delay (Sec)	Power (Watt)	PDP (Joules)
MOSFET	2.5886E-09	2.0751E-02	5.3716E-11
CNTFET	2.9259E-09	1.0562E-05	3.090E-14

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Figure 5 shows Delay in implementing Synchronizer using CNTFET and MOSFET. As seen in the figure, delay is nearly the same in both the configurations.

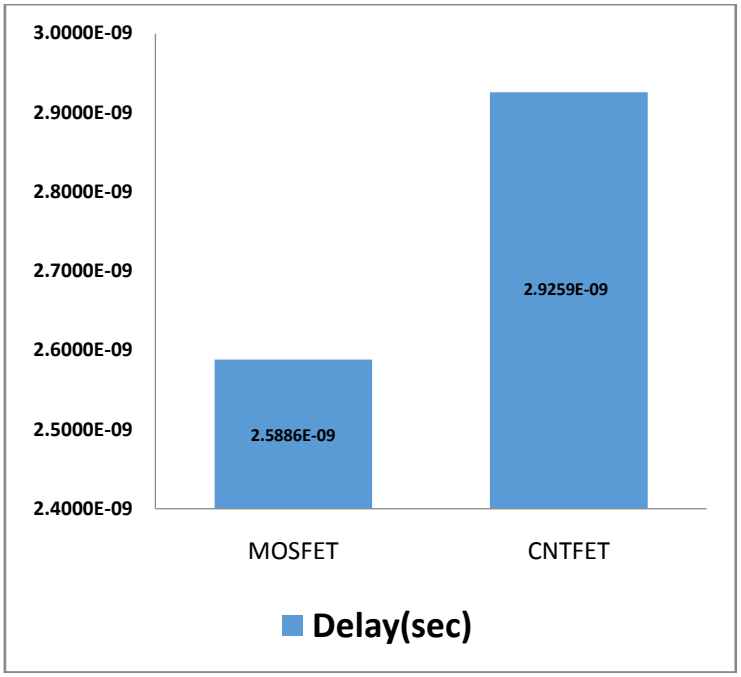

Figure 5: Comparison of Delay for MOSFET and CNTFET

Figure 6 shows Average power consumption in implementing Synchronizer using CNTFET and MOSFET. It clearly shows that average power in CNTFET is lower than in case of MOSFET.

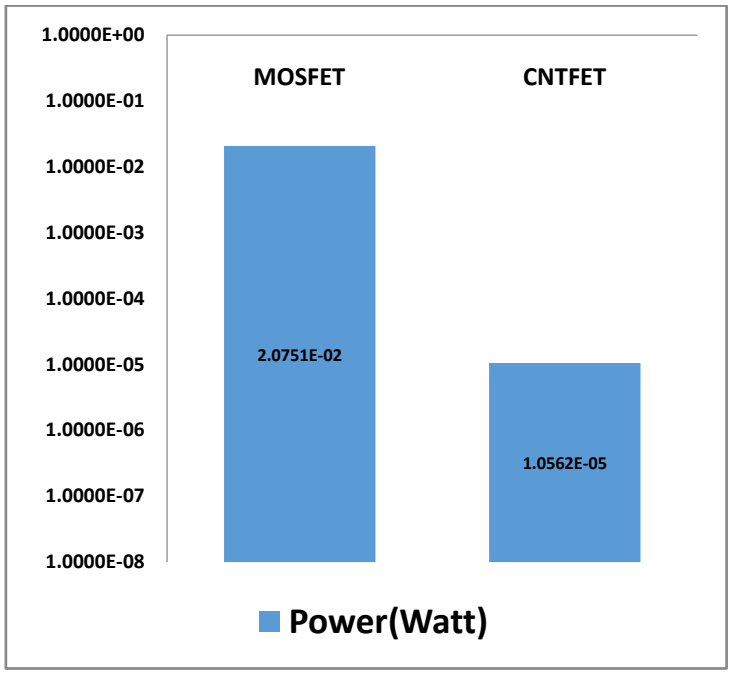

Figure 6: Comparison of Average Power for MOSFET and CNTFET.

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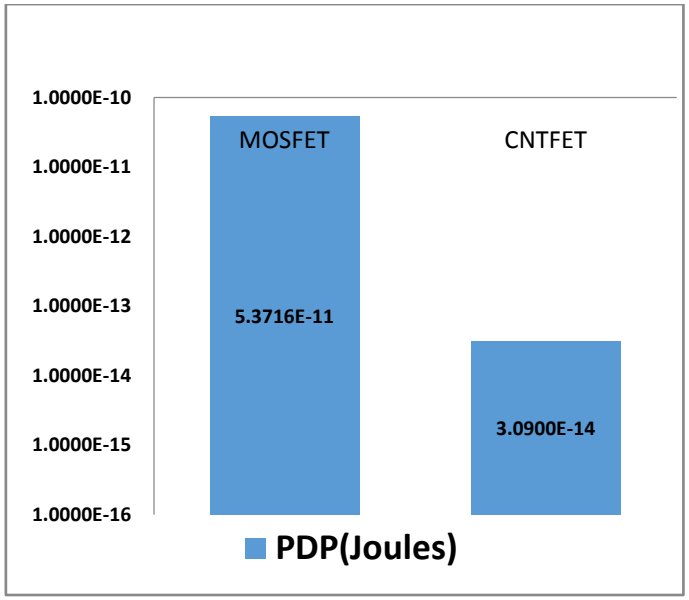

Figure 7: Comparison of PDP for MOSFET and CNTFET

Voltage Variation:

The reduction in power consumption due to voltage scaling is also confronted with the increased sensitivity to voltage variations; this is a major concern to assess the performance of a new technology such as CNTFETs. Figures 8 show the PDP for 32nm MOSFET and CNTFET synchronizer, respectively when the supply voltage is decreased until the gate stops functioning. This show that the synchronizer operate until the supply voltage decreases to 0.5 V and 0.6 V, respectively. Even though the PDP is changed depending on the supply voltage, the change of PDP in a CNTFET is less than a MOSFET because a CNTFET has a lower gate capacitance and a higher mobility than a MOSFET.

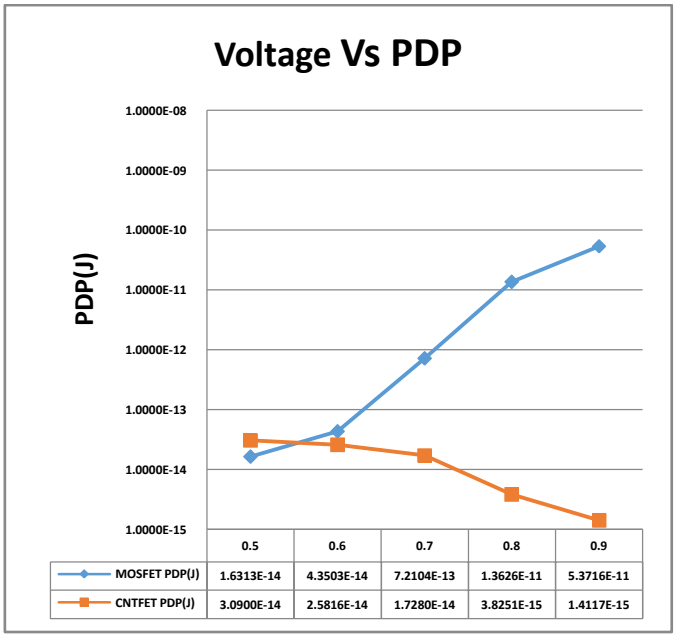

Figure 8: Voltage vs. PDP for 32nm CNTFET and MOSFET based synchronizer

Temperature Variation:

As the circuit speed increases, larger power consumption is often encountered, thus resulting in more heat at chip level. Circuits with excessive power dissipation are more susceptible to run-time failures and account for serious reliability problems. Figure 9 show that the PDP of the MOSFET circuit increases with temperature; however, the PDP of the CNTFET circuit is constant due to the high thermal stability of CNFETs.

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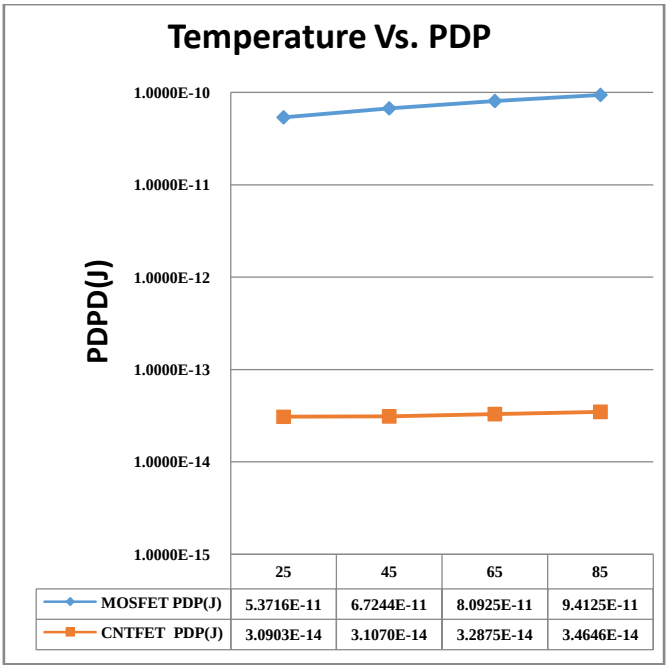

CONCLUSION

Metastability occurs when signals are transferred between asynchronous clock domains. This can be avoided by using sequential circuit. In this paper, we presented sequential circuit using CNTFET and MOSFET and simulated in HSPICE 32nm technology. From the analysis it can be seen that CNTFET exhibit the best metastable response as compare to MOSFET. This device has a very short critical time window, thus reducing the probability that they will go into a metastable state. Apart from this, CNTFET based flip-flop will return to a stable state much faster if they have gone metastable. The CNTFET based circuit has better noise immunity, less delay and less avg. power as compare to MOSFET. The PDP of CNTFET is almost constant for low voltages and at high temperatures while in MOSFET PDP increases linearly. Noise immunity is also better in case of CNTFET. The quantitative results of this paper have confirmed that CNTFET technology is a viable solution to replace conventional CMOS technology and it turns out to be an effective choice of future technology if manufacturability issues such as controllability of metallic/semiconducting property and metallic contacts are taken care of.

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